AMENDMENTS TO THE CLAIMS:

Claims 4-11, 13, 15-18, 20, and 22-25 (canceled without prejudice)

1. (currently amended) A method of fabricating a CMOS circuit ~~fabricated using a process that can create~~ comprising thick oxide transistors and thin oxide transistors by a fabrication process, said method comprising:

fabricating a differential logic circuit ~~fabricated of~~ having a plurality of thin oxide transistors~~,~~ and having a plurality of logic inputs by the fabrication process; and

fabricating a current source, ~~supplying~~ operable to supply bias current to the differential logic circuit, ~~the current source fabricated using~~ comprising at least one thick oxide transistor by the fabrication process.

2. (currently amended) The ~~apparatus~~ method according to claim 1, wherein the current source has a control input that can determine how much current is available to source to the differential logic circuit.

3. (currently amended) The ~~apparatus~~ method according to claim 2, further comprising an adaptive bias control that provides a control signal at the control input of the current source to increase the bias current available to the differential logic circuit.

12. (currently amended) A method of fabricating by a fabrication process a CMOS circuit ~~fabricated using a process that can create~~ comprising thick oxide transistors and thin oxide transistors, said method comprising:

fabricating by the fabrication process a differential logic circuit ~~fabricated~~ comprising a plurality of thin oxide transistors, and having a plurality of inputs;

fabricating by the fabrication process a current source, ~~supplying~~ operable to supply bias current to the differential logic circuit, the current source fabricated using at least one thick oxide transistor, the current source having a control input that can determine how much current is available to source to the differential logic circuit; and

fabricating by the fabrication process an adaptive bias control that provides a control signal at the control input of the current source to selectively control the bias current available to the differential logic circuit.

14. (currently amended) The ~~apparatus~~ method according to claim 12, further comprising a bias load circuit loading the differential logic circuit.

19. (currently amended) A method of fabricating a CMOS circuit ~~fabricated~~ using a process that can create thick oxide transistors and thin oxide transistors, comprising:

fabricating by the process a differential logic circuit ~~fabricated of~~ comprising a plurality of thin oxide transistors, and having a plurality of inputs, the differential logic circuit further comprising a pair of matched thin oxide transistors configured as a differential inverter;

fabricating by the process a current source, ~~supplying~~ operable to supply bias current to the differential logic circuit, the current source comprising a thick oxide transistor receiving a supply voltage at a drain thereof and coupling a reduced supply voltage to the differential logic circuit through a source thereof, the current source

having a control input at a gate thereof that can determine how much current is available to source to the differential logic circuit; and

fabricating by the process an adaptive bias control that provides a control signal at the control input of the current source to selectively control the bias current available to the differential logic circuit.

21. (currently amended) The ~~apparatus~~ method according to claim 19, further comprising a bias load circuit loading the differential logic circuit.

26. (new claim) The method according to claim 1, wherein the plurality of thin oxide transistors of the differential logic circuit fabricated by the fabrication process are each characterized as having a higher switching speed and a higher transconductance gm than the at least one thick oxide transistor of the current source fabricated by the fabrication process.

27. (new claim) The method according to claim 1, wherein the at least one thick oxide transistor fabricated by the fabrication process is operable to operate in a higher voltage condition than can the plurality of thin oxide transistors fabricated by the fabrication process and is further characterized as being larger and slower in operation than the plurality of thin oxide transistors.

28. (new claim) The method according to claim 12, wherein the plurality of thin oxide transistors of the differential logic circuit fabricated by the fabrication process are each characterized as having a higher switching speed and a higher

transconductance gm than the at least one thick oxide transistor of the current source fabricated by the fabrication process.

29. (new claim) The method according to claim 12, wherein the at least one thick oxide transistor fabricated by the fabrication process is operable to operate in a higher voltage condition than can the plurality of thin oxide transistors fabricated by the fabrication process and is further characterized as being larger and slower in operation than the plurality of thin oxide transistors.

30. (new claim) The method according to claim 19, wherein the plurality of thin oxide transistors of the differential logic circuit fabricated by the process are each characterized as having a higher switching speed and a higher transconductance gm than the at least one thick oxide transistor of the current source fabricated by the process.

31. (new claim) The method according to claim 19, wherein the at least one thick oxide transistor fabricated by the process is operable to operate in a higher voltage condition than can the plurality of thin oxide transistors fabricated by the process and is further characterized as being larger and slower in operation than the plurality of thin oxide transistors.